Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**3 2 1 24 23 22 21**

**10 11 12 13 14**

**4**

**5**

**6**

**7**

**8**

**9**

**20**

**19**

**18**

**17**

**16**

**15**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref: 4543Y**

**APPROVED BY: DK DIE SIZE .087” X .091” DATE: 10/13/21**

**MFG: IDT THICKNESS .000” P/N: 54HCT543**

**DG 10.1.2**

#### Rev B, 7/1